Abstract of the Disclosure

A memory device to perform an erase operation algorithm that specifically deals with different types of defects in a memory array. The memory array of one embodiment of the present invention has primary and redundant elements. A register is used for each redundant element to store the address of a defective primary element and an error code that indicates the type of defect in the defective primary element. Control circuitry is used to control memory operations to the memory array. The control circuitry performs an erase operation algorithm that is specific to an error code when a defective primary element is addressed during an erase operation.